CLAIMS

1. A semiconductor memory card used by being connected to an access unit, comprising:

a host interface section which sends a control signal and data to said access unit and receives a signal from said access unit;

a nonvolatile memory which includes a plurality of nonvolatile memory chips and in which a plurality of continuous sectors is grouped to be a block as a minimum unit of data erasing;

a memory controller which controls erasing, writing, and reading of data with respect to said nonvolatile memory; and

a host information memory which temporarily stores a data write start address and a data size value given by said access unit, wherein

said memory controller includes a free physical area generation section which determines whether or not to perform erasing of invalid blocks of said nonvolatile memory based on the data write start address and the data size value temporarily stored in said host information memory, and simultaneously performs writing of data to one nonvolatile memory chip and erasing of blocks of another nonvolatile memory chip when performing erasing of said invalid blocks.

2. The semiconductor memory card according to claim 1, wherein said free physical area generation section determines the number of blocks to be erased so that an erase time corresponds to a write time of write data.

3. The semiconductor memory card according to claim 1, wherein said memory controller is connected to each of said plurality of nonvolatile memory chips with respectively independent bidirectional buses.

4. The semiconductor memory card according to claim 1, wherein said nonvolatile memory is composed of two nonvolatile memory chips in which, while a write process is performed in one nonvolatile memory chip, erasing of invalid blocks is performed in the other nonvolatile memory chip.

5. A semiconductor memory control apparatus used by being connected to a nonvolatile memory which includes a plurality of nonvolatile memory chips and in which a plurality of continuous sectors is grouped to be a block as a minimum unit of data erasing:

a host interface section which sends a control signal and data to an access unit and receives a signal from said access unit;

a memory controller which controls erasing, writing, and

reading of data with respect to said nonvolatile memory; and

a host information memory which temporarily stores a data write start address and a data size value given by said access unit, wherein

said memory controller includes a free physical area generation section which determines whether or not to perform erasing of invalid blocks of said nonvolatile memory based on the data write start address and the data size value temporarily stored in said host information memory, and simultaneously performs writing of data to one nonvolatile memory chip and erasing of blocks of another nonvolatile memory chip when performing erasing of said invalid blocks.

6. The semiconductor memory control apparatus according to claim 5, wherein said free physical area generation section determines the number of blocks to be erased so that an erase time corresponds to a write time of write data.

7. The semiconductor memory control apparatus according to claim 5, wherein said memory controller is connected to each of said plurality of nonvolatile memory chips with respectively independent bidirectional buses.

8. The semiconductor memory control apparatus according to claim 5, wherein said nonvolatile memory is composed of two

nonvolatile memory chips in which, while a write process is performed in one nonvolatile memory chip, erasing of invalid blocks is performed in the other nonvolatile memory chip.

9. A semiconductor memory control method in a semiconductor memory card having a nonvolatile memory which includes a plurality of nonvolatile memory chips and in which a plurality of continuous sectors is grouped to be a block as a minimum unit of data erasing, said semiconductor memory control method comprising the steps of:

temporarily storing a data write start address and a data size value given by an access unit in a host information memory;

determining whether or not to perform erasing of invalid blocks of said nonvolatile memory based on the data write start address and the data size value temporarily stored in said host information memory; and

simultaneously performing writing of data to one nonvolatile memory chip and erasing of blocks of another nonvolatile memory chip when performing erasing of said invalid blocks.

10. The semiconductor memory control method according to claim 9, further comprising the step of determining the number of blocks to be erase so that an erase time corresponds to a

write time of write data when erasing of invalid blocks of said nonvolatile memory is performed.

11. The semiconductor memory control method according to claim 9, said nonvolatile memory is composed of two nonvolatile memory chips in which, while a write process is performed in one nonvolatile memory chip, erasing of an invalid block is performed in the other nonvolatile memory chip.